Role of the CPU components in the Fetch-decode-execute cycle

S.P.I.R.I.T
- ✓ **Independence**
- ✓ **Perseverance**

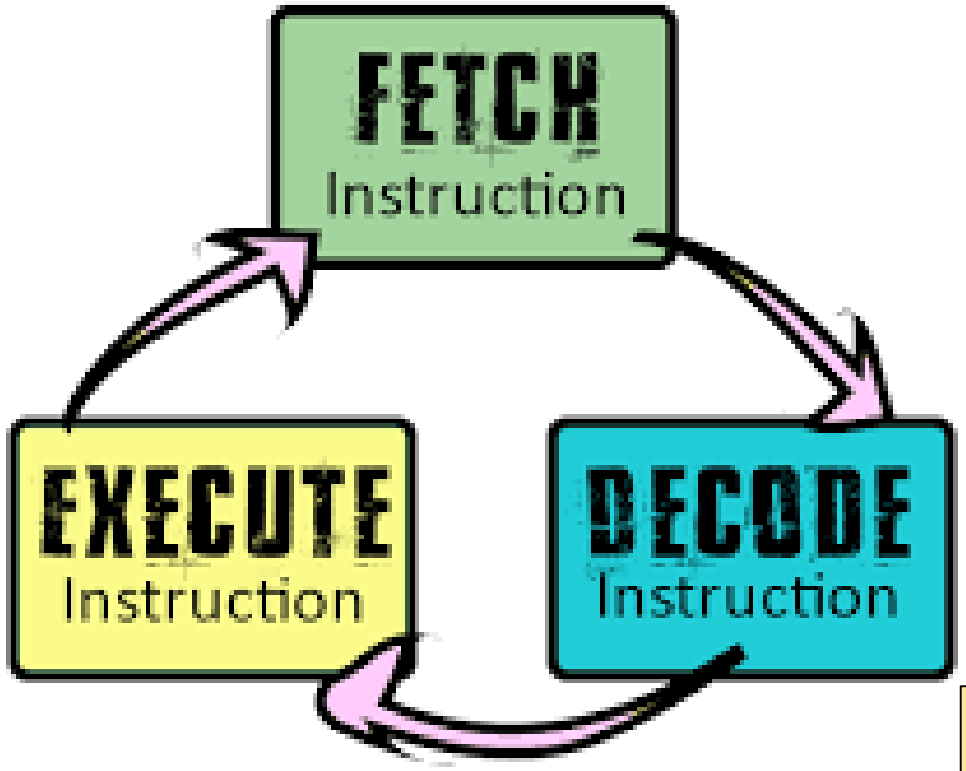
Monday, 04 April 2022

Learning Intention

To develop knowledge by explaining what buses are in computer systems

To secure understanding by identifying the key concepts in the F-D-E cycle

To achieve excellence by identifying the roles that different registers play in the F-D-E cycle



Keywords

Tier 2 words:
Retrieve
To get or bring something back from somewhere

Tier 3 word:
Bus
used to connect **computer** components and transfer data between them.

Buses

The control bus is used by the controller to send control signals to different parts of the computer.

The address bus - When data is saved or loaded from memory, the address at which it is to be stored or loaded from must be sent. The storage address of data always travels along an address bus.

The data bus - Data will then need to be moved between several parts of a computer. The path along which data travels is called a data bus.

See the animation in the resource folder:

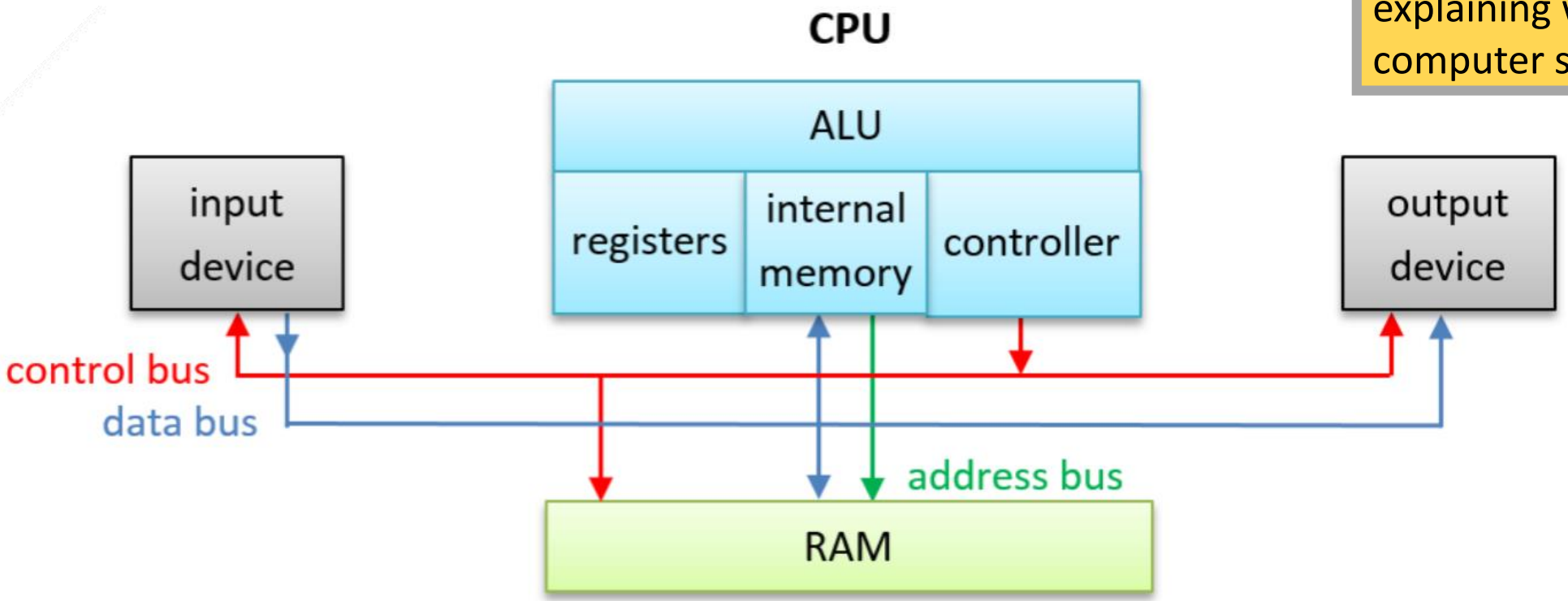
1.2.b Components of the CPU.swf

To develop knowledge by explaining what buses are in computer systems

Task 1 – Draw the diagram – 5 minutes

Draw the Diagram.

To develop knowledge by explaining what buses are in computer systems



Components of the CPU: controller, arithmetic and logic unit (ALU), internal memory, registers, buses

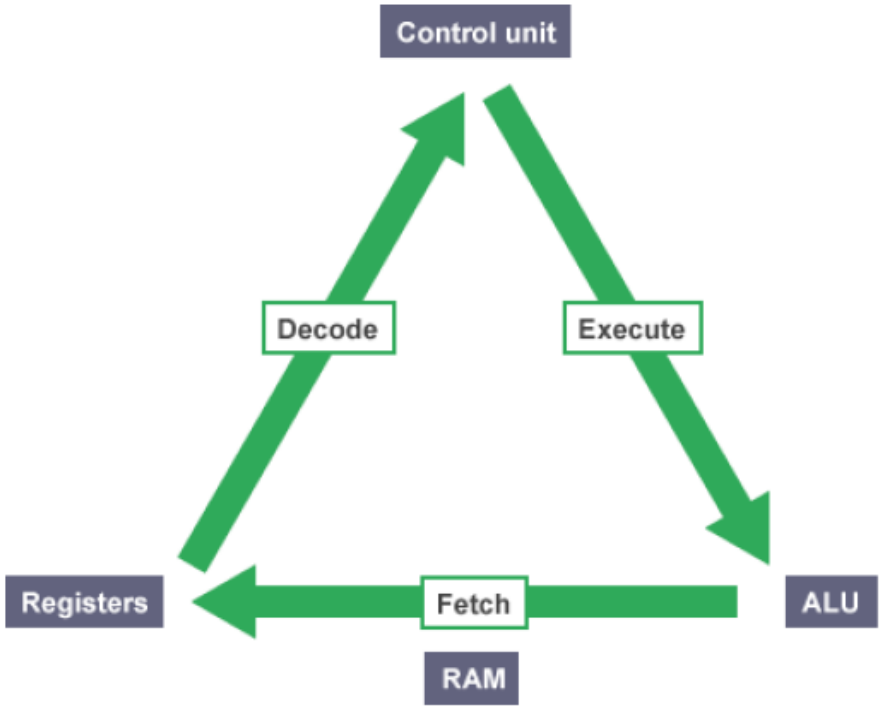
Fetch-decode–execute cycle

Watch the video on the Fetch –decode - Execute cycle
https://www.bbc.co.uk/bitesize/guides/zhppfcw/revision/4

To secure understanding
by identifying the key concepts in the F-D-E cycle

There are **three** steps to processing instructions given by a currently running program:

Fetch-decode-execute cycle
This is the process the processor follows to retrieve instructions from memory
It decodes what to do and then carries out the actions.



https://www.futurelearn.com/courses/how-computers-work/0/steps/49284

WJEC Definitions

There are **three** steps to processing instructions given by a currently running program:

Fetch:

The fetch cycle takes the address required from memory, stores it in the instruction register, and moves the **program counter** on one so that it points at the next instruction.

Simple version

FETCH: Control Unit *fetches* instructions from main memory (RAM) and **stores it temporarily in the registers**

Decode:

The control unit checks the instruction in the instruction register. The instruction is decoded to determine the action that needs to be carried out.

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Execute:

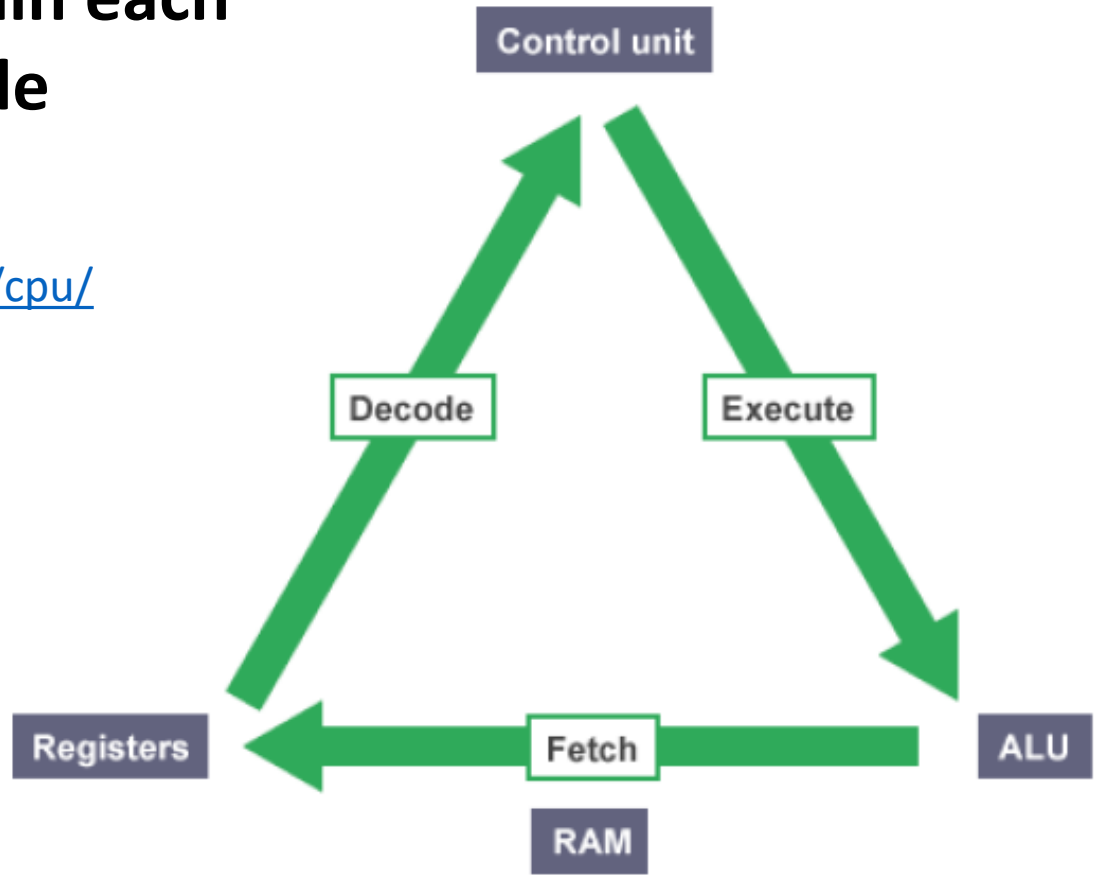
The actual actions that happen during the execution cycle depend on the instruction itself.

Task 2

1. Copy the Fetch – execute cycle diagram.

2. Use WJEC info and the link to explain each step of the Fetch-decode-execute cycle

http://www.teach-ict.com/gcse_computing/ocr/212_computing_hardware/cpu/miniweb/pg3.php



Registers used

To achieve excellence by identifying the roles that different registers play in the F-D-E cycle

To secure understanding by identifying the key concepts in the F-D-E cycle

Program Counter (PC) – a counter that keeps track of the memory address of which instruction is to be executed next.
The program counter increments (adds 1 on) each time the cycle runs

Accumulator – a small holding area in the ALU which temporarily holds the result of the Instruction

Memory Address Register (MAR) – the address in ma t is currently being read or written. The memory address stored in the PC is transferred to the MAR

Memory Data Register (MDR) holds the contents/data found at the address held in the MAR when being transferred from memory to CPU (and vice versa)

Current Instruction register (CIR) – Stores the instruction that has just been fetched from memory which is currently being executed.

Instructions

Registers used – (teacher)

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FETCH

The instruction or data held in the MDR is copied into the current instruction register (CIR).

PC 1

MAR

MDR

Instruction1

CIR

RAM

Address location 0	Address location 1	Address location 2	Address location 3
Instruction1	Instruction2	Instruction3	

The cycle then repeats

DECODE

Controller decodes (works out) instruction

?

EXECUTE

The instruction is then executed (carried out)

The result of the process is stored in the Accumulator

Result

ACC

The result may also need to be stored back into memory

Registers used

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FETCH

PC 2

MAR 0

MDR

Instruction2

CIR

RAM

Address location 0	Address location 1	Address location 2	Address location 3
Instruction1	Instruction2	Instruction3	

The cycle then repeats until all instructions are complete

DECODE

Controller decodes (works out) instruction

?

EXECUTE

The instruction is then executed (carried out)

The result of the process is stored in the Accumulator

Result

ACC

The result may also need to be stored back into memory

Using registers for top marks

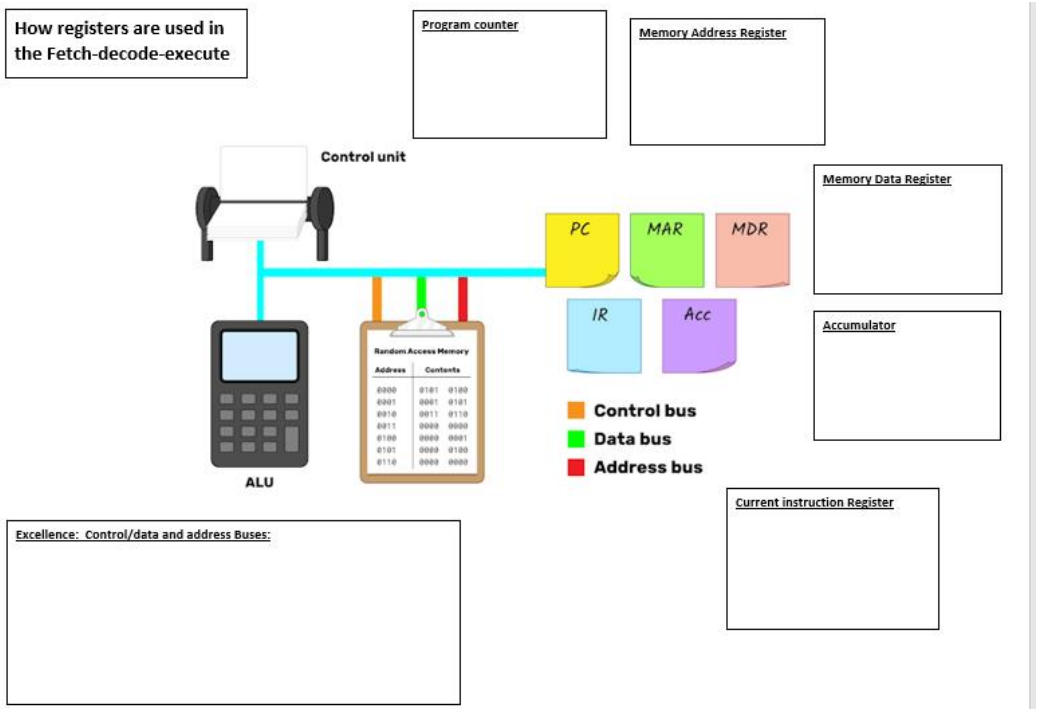
1. The **memory** address held in the program counter (PC) is copied into the memory address register (MAR).
2. The address in the program counter is incremented (increased) by one. The program counter now holds the address of the next **instruction** to be **fetched**.
3. The processor sends a signal along the address **bus** to the memory address held in the MAR.
4. The instruction or **data** held in that memory address is sent along the data bus to the memory data register (MDR).
5. The instruction or data held in the MDR is copied into the current instruction register (CIR).
6. The instruction or data held in the CIR is **decoded by the controller** and then **executed**. Results of processing are stored in the **accumulator (ACC)**.
7. The cycle returns to step one.

https://www.101computing.net/LMC/ - to show step by step FDE cycle

To achieve excellence by identifying the roles that different registers play in the F-D-E cycle

Registers Task

1. Glue in the register sheet and complete the descriptions for each register



Think it

Research the how data moves between the following hardware during the Fetch-Decode-Execute cycle

CPU - Hard disk - RAM